Development of a Transponder for the ISTNanoSAT (October 2015)

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***Abstract*—This paper focus on the implementation of a functional prototype for the digital signal processing of an intermediate frequency (10.7 MHz), Binary Phase Shit Keying (BPSK) received.**

For this prototype a physical system was build using an analog-to-digital and digital-to-analog integrated circuits and glue logic. This system was connected to a Nexys 4 board, based on the Artix-7 Field Programmable Gate Array (FPGA).

This FPGA allowed to build the necessary hardware and its reconfiguration for the radio frequency signal processing.

***Index Terms*—FGPA, transponder, BPSK**

I. Introduction

THIS work focus on a sector of the hardware to be used in the project and construction of a digital transponder. This paper presents one of the possible solutions for the implementation of BPSK received using reconfigurable hardware and a new developed interface hardware.

A. Motivation and Goals

The nano-satellite digital communications module a transponder. The module development is made in a continuous and progressive way. So, the following objectives were proposed:

- Development of a data acquisition system aimed to interconnect a FPGA and an Analog-Digital Converter (ADC);
- Implementation of a BPSK receiver on a reconfigurable hardware;
- Design the data output system, digital-analog converter;
- Allow the connection to a digital signal processor;
- Implement a functional prototype;
- Implement a BPSK transmitter in intermediate frequency.

B. Summary of the work and its results

The project's central element is the Digital Signal Processing using a FPGA borad. The choice for this borad was a Digilent development board named Nexys 4. The communications module will receive data through the radio frequency analog signal. As a central element can only process digital data it was necessary to implement a module for both designed acquisition and analog transmission.

The acquisition sending modules were projected to work at the intermediate frequency of 10.7 MHz and baseband. So it is possible to receive and send the information of the radio frequency analog signal.

II. System Theory

A. Model of the Transponder

The architecture of a classic transponder is shown in the Fig. 1 were we can see two main parts: the analog hardware and the digital model.

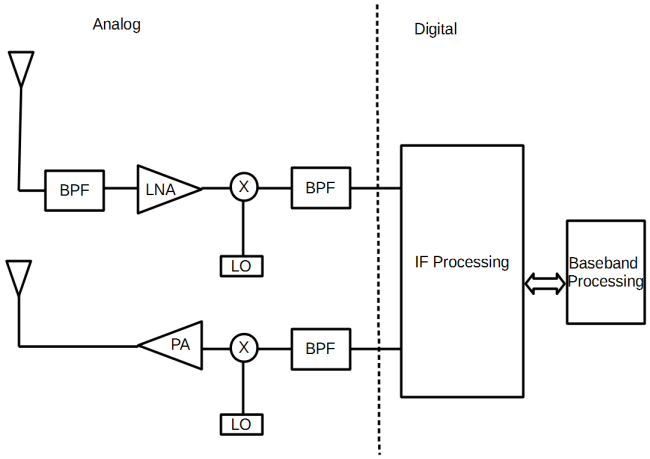

Fig. 1: Classical transponder architecture.

The analog radio frequency block is responsible for the capture and conditioning of the radio signal in the reception and emission. At the end of the chain, we have the radio frequency on an intermediate frequency of 21.4 MHz or 10.7 MHz.

The latest transponder satellites come equipped with a Software Defined Radio (SDR) type system based on a FPGA, for example S9107 SDR Space Transponder.

The FPGA allows faster processing because of it's parallel processing capability, but for applications with complex algorithms it is more difficult for implementation, and a Digital Signal Processor (DSP) is better choice.

B. Subsampling

The subsampling follows theory of sampling for passband. The passband sampling thorem is equation (1), where f_c is central frequency, LB is the bandwidth and m is a integrator.

$$\frac{2}{m}(f_c - \frac{LB}{2}) < f_s \leq \frac{2}{m-1}(f_c + \frac{LB}{2}),\ com\ m = 1, 2, ... \tag{1}$$

This sampling technique uses the spectral images that are generated by the sampler on the sampling process. The periodic sampling is twice faster than the bandwidth of the signal. It is necessary that the ADC has enough analog bandwidth to process the bandpass signal.

Equation (2) allows to obtain the values of the replicas generated by sampler.

$$f_{c2} = f_c - kf_s \tag{2}$$

Where k is a integer.

C. Frequency Plan

The BPSK receiver captures the signal with $f_c = 10.7$ MHz carrier at a binary rate of 130 kbit/s.

The case in which the order of $k = 5$ replica gives the signal of interest, centered at 250 kHz.

Fig. (2) shows a graphical form of the work frequency the receiver using sub-sampling.

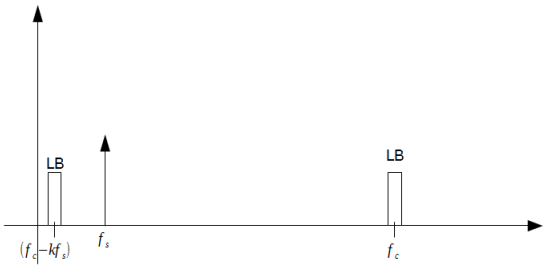

Fig. 2: Frenquency plan, center of the subsmapling receiver.

D. CIC filter and Decimation

The Cascaded IntegratorComb (CIC) filters are digital filters of easy implementation and low required computing resources, only sums and delays. They reveal themselves as very efficient digital filters for narrow bandwidth.

CIC filters can be used an anti-aliasing filter decimation structures, often employed in SDR receivers.

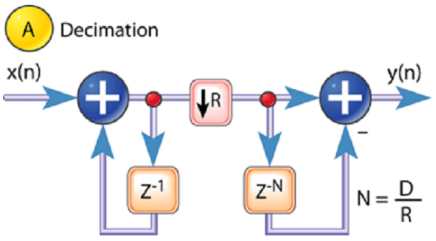

Fig. 3: CIC Decimator [4].

The digital decimator in the Fig. 3 does not require any complex system to store samples. In the block decimation as shown in the image allows reducing the store for line delay because that block works at the lowest sampling frequency.

E. Transmitter BPSK

The BPSK transmitter is a binary modulator (contains two symbols). The information is carried in phase. That change is done in the interval 0^o and 180^o degrees.

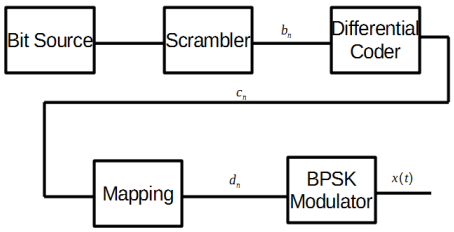

Fig. 4: Block diagram of the BPSK transmitter.

The BPSK modulator internally generates the carrier for the BPSK signal. Equation (3) is a model to implement a signal generator BPSK, the d_n is the data to be transmitted. The value of d_n is either 1 or -1.

$$x(t) = d_n \sin(2\pi f_o t) \tag{3}$$

F. Costas Loop Receiver

The Costas Loop is a receiver that can be used to demodulate BPSk signals (fig. 5) and is based on phase-locked loops, which are used to retrieve the phase information contained in the modulated signal $x(t)$.

The receiver allows simultaneously synchronization with the frequency of the carrier.

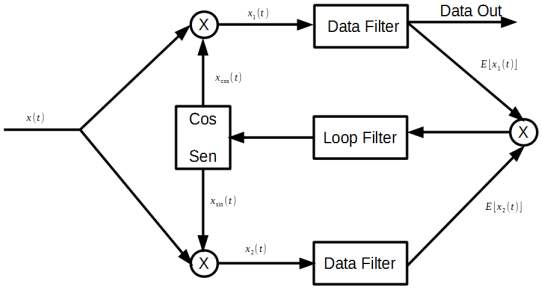

Fig. 5: Costas Loop.

The Costa Loop has an oscillator and this oscillator has a digital control. It generates two signals, a cosine and a sine for to multiplier. Fig. 6 shows the model of a Numerically Controlled Oscillator.

An integrator is used in the ramp with 18 information bits and the 6 most significant bits of this ramp are used to index values contained in the sine and cosine table, described by the equations (4) and (5).

$$x_{sin} = \sin(2\pi - \frac{2\pi n}{64}), n = 1, 2, 3...64 \tag{4}$$

$$x_{cos} = \cos(2\pi - \frac{2\pi n}{64}), n = 1, 2, 3...64 \tag{5}$$

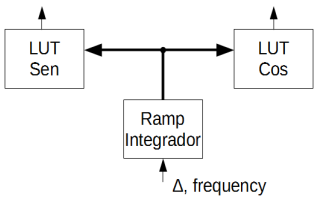

Fig. 6: Numerically controlled oscillator, model.

With the sine and cosine functions defined in tables, now is important to analyse the working frequencies for Numerator Controlled Oscillator (NCO). To meet the correct operation of the receiver, the NCO must have a clock frequency of 1.045 MHz and generate a core frequency of 250 kHz.

As already been reported for the oscillator control of sine and cosine functions, they are used in an integrator ramp, and thus to generate a sine or cosine function it is necessary to know the frequency jump of the ramp at every updating the frequency of work, based on the equation (6).

$$\Delta_{osc} = \frac{2 \times (2^{17} - 1) \times f_{osc}}{f_s} \tag{6}$$

The complex multiplier performs the operation of input signal multiplication with the generated signal the NCO.

$$x_{cos}(t) = \cos(2\pi f_0 t + \phi_0) \tag{7}$$

$$x_{sin}(t) = \sin(2\pi f_0 t + \phi_0) \tag{8}$$

It can be shown that the output of the low pass filters of each of the arms in the real arm is $E[x_{cos}(t)]$ the demodulated signal plus the variation of the signal phase, the imaginary arm is $E[x_{sin}(t)]$, the value of the variation of the signal phase. The complex multiplier works as a phase detector.

When synchronization is archived the frequency of the NCO is equal to the carrier frequency.

III. System Architecture

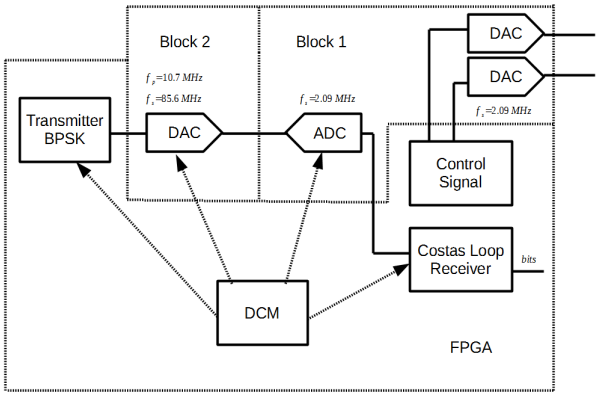

Fig. 7: Block diagram, transponder.

The hardware Block 1 contains an ADC with two channels and two digital to analog converter (Digital-Analog Converter (DAC)) that allows the visualization of internal signals of the receiver Costas Loop along the chain.

Block 2 only supports digital-to-analog conversion.

The FPGA is the brain of all operations of the transponder (processor IF), ie, it does the management of clocks through the function block Digital Clock Management (DCM), digitally creates the BPSK signal and controllers all processes in the receiver.

A. Analog and Digital Module

In the implementation of this work it was necessary to create a new module on hardware that allows to communicate with the real world (analog) and interact with the FPGA. So this was the first challenge of the work, to find the integrated circuits that allow this communication between the digital world and the analog world.

Block 2 uses the same features that Block 1, ie uses the same printed circuit board, but only an output analog circuit is available.

As a first goal, it was proposed an ADC that allow to extract samples of the 10.7 MHz IF with no loss of information. Thus it is considered the choice of an ADC without frequency sampling process less than 65 MSample/s with 12-bit parallel interface. On the DAC the number of bits, but the speed would be above 65 Msample/s.

B. Test Digital-Analogue

The test clocks shown in Fig. 8 allows the test in full scale of the ADC, ie clock frequency is 65 MHz in all digital circuits.

The bus used to interconnect the ADC and DAC is same. This control there was no digital processing, ie, the bits on the ADC were sent directly DAC.

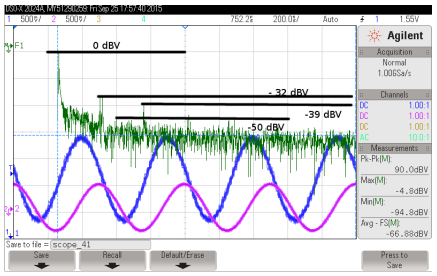

Fig. 8: FFT of output DAC signal

Fig. 4.11 shows the spectral analysis (Fast Fourier Transform (FFT)) of the output. Reading the signals we see that the Signal SNR is approximately 50 dB and it is possible end to see the value of two harmonicas with -32 dBV and -39 dBV.

C. Prototype

The prototype has 3 modules, as shown in Fig. 9. We can identify the modules of emission on the left photo and the receiver module in the right.

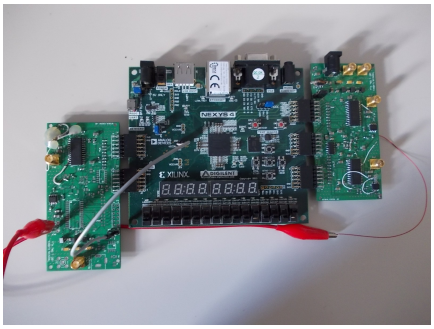

Fig. 9: Prototype photograph

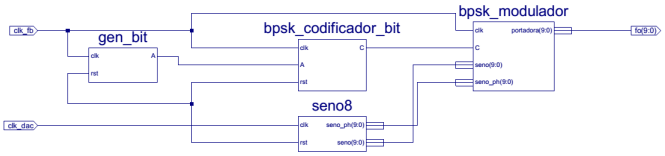

Fig. 10: Model transmitter BPSK.

D. Transmitter

The BPSK transmitter has a carrier frequency in 10.7MHz with 500 mV_{pp}. The sampling frequency is 85.6 MHz (DAC output) and the bit rate is 130 kbit/s. The sinusoidal carrier was represented by a 10 bit LUT.

E. Costas Loop Receiver

The first element of the digital signal processing is the CIC decimator filter. The signal is coming from the ADC as digital 10 bit two's complement words. The output of the CIC has a digital words of 11 bit.

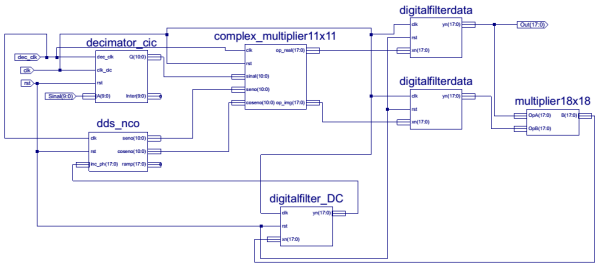

Fig. 11: Costas Loop Receiver

The NCO project has a central frequency of 242.625 kHz and the sine and cosine a width of 11 bits.

The data filter is an Infinite Impulse Response (IIR) filter with one pole in 130 kHz. The digital filter uses 18 bit words.

F. Artix-7 FPGA

Table I show summarizes the resources used in the implementation of the transmitter and receiver in an Artix-7 FPGA chip.

Device	Used	Available	Total Used (%)
Register	245	126 800	1
Slices LUT	258	63 400	1
Slices	98	15 850	1
IOB	55	210	26
DSP48E1s	9	240	3

TABLE I: Report, Artix-7

IV. Test and Results

The Fig. 12 shows the of the signal FFT, after sampling.

After the FFT analysis of the signal is possible to verify the signal replicas generated. The replicas of order 5, 6, 4, 7 and 3 are centred at frequencies 250 kHz, 1.84 MHz, 2.34 MHz, 3.93 MHz and 4.43 MHz, respectively.

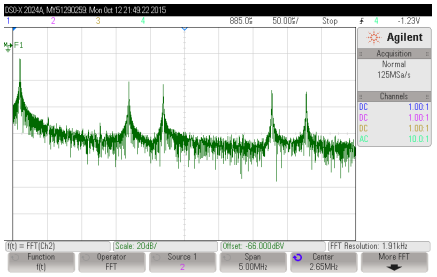

Fig. 12: Spectrum of signal after sampling.

The FFT on the Fig. 13 shows a spectrum of the BPSK signal (random) bits at the transmitter with a carrier frequency of 10.692 MHz and a binary rate of 130.625 kbit/s.

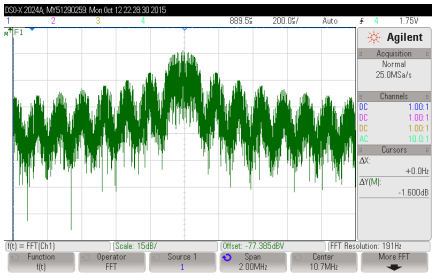

Fig. 13: Spectrum of transmitter.

The next result is shown in Fig. 14. Analyzing the spectrum it is possible to identify the original BPSK signal, centred at 242 kHz.

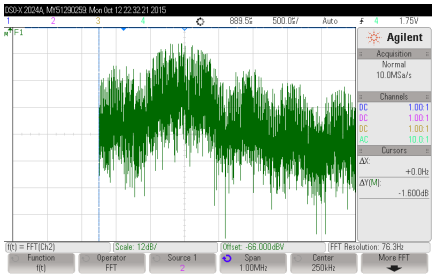

Fig. 14: Spectrum of sampling BPSK signal.

Fig. 15 shows the BPSK signal at the output of the decimator. The effect of the CIC filter is visible as a detection the bandwidth, ie, a kind of low pass filter.

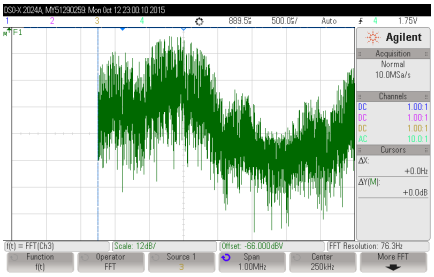

Fig. 15: BPSK signal after the decimator.

In the last test, the result are shown of the Fig. 16.

The output of the real arm allows a correct of the BPSK signal as evidenced by the measured value in the oscilloscope and presented in the figure.

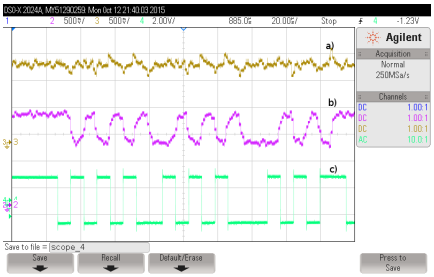

Fig. 16: BPSK signal: a) imaginary arm, b) real arm and c) differential coder from transmitter.

V. Conclusion

The hardware module designed to work together with the development board Nexys 4,lets one have a number of options for the acquisition of analog signals, digital signal processing and digital or analog transmit signals.

Due to technical limitations, it was not possible to have both data converters connected independently, so there was a sharing of the 10 bit data bus between the ADC, DAC and FPGA. While knowing that the circuit behaviour would be much better without the sharing of data between ADC and DAC without this condition it would not be possible to think of the solution to develop a receiver using subsampling.

The implementation result are present show that the system performs as expected and is ready for integration in the ISTNanoSAT transponder.

References

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